

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus generally comprising a first data modification circuit and a composite circuit. The first data modification circuit may be configured to generate a first output data stream in response to performing a first modification on at least one first image from a first input data stream. The composite circuit may be configured to generate a combined output data stream in response to performing a spatial combination of the first output data stream and a second output data stream.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and the new claims can be found in the specification, for example, on page 3 lines 14-16, page 6 lines 3-11, page 7 lines 7-11, page 7 line 17 thru page 8 line 16 and FIGS. 1-2 as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 6 under 35 U.S.C. §112, first paragraph, has been obviated by appropriate amendment and should be withdrawn. Claim 6 has been cancelled.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 9-11, 13 and 18-19 under 35 U.S.C. §102(e) as being anticipated by Zhang et al. '711 (hereafter Zhang) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 1, 4, 5, 12-15 and 20 under 35 U.S.C. §102(e) as being anticipated by Porter '354 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 1, 7, 8, 13, 16 and 17 under 35 U.S.C. §102(e) as being anticipated by Moreton et al. '729 (hereafter Moreton) has been obviated by appropriate amendment and should be withdrawn.

Zhang concerns a system and method for transporting a compressed video and data bit stream over a communication channel (Title). Porter concerns a method and apparatus for displaying multiple graphics images in a mixed video graphics display (Title). Moreton concerns a circuit to separate and combine color space component data of a video image (Title). Each of Zhang, Porter and Moreton do not appear to disclose or suggest every element as arranged in the claims. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 provides a composite circuit configured to generate a combined output data stream in response to performing a

spatial combination of a first output data stream and a second output data stream. In contrast, each of Zhang and Moreton appear to be silent regarding spatial combinations of two data streams. Therefore, Zhang and Moreton each do not appear to disclose or suggest a composite circuit configured to generate a combined output data stream in response to performing a spatial combination of a first output data stream and a second output data stream as presently claimed.

Claim 1 further provides a first data modification circuit configured to generate a first output data stream in response to performing a first modification on at least one first image from a first input data stream. In contrast, Porter and Moreton each appear to be silent regarding a circuit modifying one or more images from a first data stream prior to spatially combining with a second data stream. Therefore, Porter and Moreton each do not appear to disclose or suggest a first data modification circuit configured to generate a first output data stream in response to performing a first modification on at least one first image from a first input data stream as presently claimed. Claim 13 provides language similar to claim 1. As such, the claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Claim 2 provides that the apparatus forms a block modify and move engine. In contrast, Zhang appears to be silent regarding

a block modify and move engine. Therefore, Zhang does not appear to disclose or suggest an apparatus forming a block modify and move engine as presently claimed. As such, claim 2 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 3 provides a second data modification circuit configured to generate a second output data stream in response to performing a second modification on at least one second image from a second input data stream. In contrast, Zhang appears to be silent regarding any one of the modification units 404, 406, 408, 514, 516 or 518 modifying an image from a second data stream other than the video signal 420. Therefore, Zhang does not appear to disclose or suggest a second data modification circuit configured to generate a second output data stream in response to performing a second modification on at least one second image from a second input data stream as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 11 provides that a spatial combination is a bitwise logical operation on a first output data stream and a second output data stream. Despite the assertion on page 4, section 4 of the Office Action, the text in column 13, lines 1-5 of Zhang do not appear to discuss a bitwise logical combination of two data streams. Instead, the cited text of Zhang appears to discuss time division multiplexing. Therefore, Zhang does not appear to

disclose or suggest that a spatial combination is a bitwise logical operation on a first output data stream and a second output data stream as presently claimed. Claim 19 provides language similar to claim 11. As such, claims 11 and 19 are fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,
CHRISTOPHER P. MAIORANA, P.C.
Christopher P. Maiorana
Registration No. 42,829
Dated: December 16, 2003

c/o Leo Peters
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

Docket No.: 00-335 / 1496.00154